AMENDMENTS TO THE CLAIMS

Please amend Claims 1-13 as follows.

Please add new Claims 14-17 as follows.

1. (Currently amended) A method ~~for~~of simulating signals in a simulated system with a digital apparatus~~, said system being simulated comprising of subsystems and connections between said subsystems, said signals being referred to said connections~~, said method comprising~~being characterized in that~~:

representing at least one of said signals ~~being represented~~ by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said bandpass signals have~~ing~~ a different bandwidth.

2. (Currently amended) The method recited in Claim 1, wherein said system ~~being~~is an essentially electrical system.

3. (Currently amended) The method recited in Claim 1, ~~wherein said method~~ further comprising:~~being characterized in that~~ representing at least two of said signals ~~being represented~~ by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said signals have~~ing~~ a representation being different from signal to signal in either at least one carrier frequency or in at least one bandwidth for a carrier frequency common for said two signals.

4. (Currently amended) The method recited in Claim 1, further comprising ~~the step of~~ replacing at least one signal representation with at least two carriers and their bandpass signals by one substitute carrier and one substitute bandpass signal when the distance between said bandpass signals is smaller than a threshold value.

5. (Currently amended) The method recited in Claim 1, further comprising ~~the step of~~ constructing a computational graph, wherein each of said subsystems is represented by at least one computation node and each computation node has~~ving~~ a computation rule; and ~~a step of~~ scheduling the execution of said computation rules for each computation node such that for a maximum amount of computation nodes at least a sequence of computations can be performed without interruptions.

6. (Currently amended) The method recited in Claim 1, wherein said system comprises ~~of~~ at least one linear subsystem and the method further comprises~~ing the step of~~ constructing a computational graph, wherein each of said subsystems is~~are~~ represented by at least one computation node and wherein for at least said linear subsystem a plurality of computation nodes are provided, each computation node being related to a selection of the carriers in said linear subsystems input signals.

7. (Currently amended) The method recited in Claim 6, wherein the computation ~~step for each of said computation~~ nodes ~~representing said linear subsystems being~~are determined by the bandwidth of the bandpass signal, associated ~~to~~with the carrier~~;~~ and related to said computation node.

8. (Currently amended) The method recited in Claim 1, wherein ~~being characterized in that~~ said signals are simulated by executing ~~of~~ a plurality of computation rules, each computation rule being specific for each subsystem.

9. (Currently amended) The method recited in Claim 1, wherein said system comprises ~~of~~ at least one nonlinear subsystem and the method further comprises~~ing the steps of~~ selecting for said nonlinear subsystem a computation method based on combining of bandpass signals when the number of carriers in said nonlinear subsystems input signals is below a threshold value and a computation method based on Fourier transformation otherwise.

10. (Currently amended) The method recited in Claim 1, further~~wherein the method~~ comprising ~~the steps of~~: constructing a computational graph, wherein each of said subsystems is represented by at least one computation node and said connections by edges between said computation nodes; and adding of down- or upsampling nodes between at least two connected nodes having a different computation step.

11. (Currently amended) A digital apparatus for simulating signals of a simulated system, said system being simulated comprising subsystems and connections between said subsystems, said signals being referred to said connections, said apparatus comprising:

means for entering a representation of said system;

means for transforming said representation into a computational graph, said computation graph comprising at least one of computation nodes, each computation node having a computation rule;

a scheduler for scheduling the execution of said computation rules of said computation nodes in time, said scheduler being adapted for scheduling the execution of said computation rule for each computation node such that for a maximum amount of computation nodes at least a sequence of computations can be performed without interruptions;

means for execution said computation rules in the order determined by said scheduler.

12. (Currently amended) The apparatus recited in Claim 11, wherein the apparatus is further ~~being~~ adapted such that at least one of said signals is represented by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said bandpass signals have~~ing~~ a different bandwidth.

13. (Currently amended) The apparatus recited in Claim11, wherein the apparatus is further ~~being~~ adapted such that at least two of said signals are represented by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said signals have~~ing~~ a representation being different from signal to signal in either at least one carrier frequency or in at least one bandwidth for a carrier frequency common for said two signals.

14. (New) The apparatus recited in Claim 11, wherein the transforming means comprises:

means for adding decimators and interpolators;

means for splitting a node relating to a linear subcircuit into a plurality of nodes; and

means for selecting an appropriate computation method for nonlinear circuits.

15. (New) The apparatus recited in Claim 11, wherein the computation nodes comprise a plurality of nodes each having a different level of priority, and wherein the scheduler is configured to schedule the execution for the node having the highest level of priority.

16. (New) The apparatus recited in Claim 15, wherein the plurality of computation nodes comprise:

a first node which is not ready for execution;

a second node which is not in a feedback loop and ready for sample-by-sample execution;

a third node which is in a feedback loop and ready for sample-by-sample execution; and

a fourth node which is ready for vector processing.

17. (New) A digital apparatus for simulating signals in a simulated system, the apparatus comprising:

an entering section configured to enter a representation of said system;

a transforming section configured to transform the representation into a computational graph, the computation graph comprising a plurality of computation nodes, each computation node having a computation rule;

a scheduler configured to schedule the execution of the computation rules of the computation nodes in time, the scheduler being adapted to schedule the execution of the computation rule for each computation node such that for a maximum amount of computation nodes at least a sequence of computations can be performed without interruptions; and

an execution section configured to execute the computation rules in the order determined by the scheduler.